[This question paper contains 5 printed pages.]

6589 *Your Roll No.* .....

B.Sc. (Hons.) Computer Science / I Sem. B

Paper – CS 104 : DIGITAL ELECTRONICS

(Admissions of 2001 to 2009)

Time : 3 Hours *Maximum Marks : 75*

(Write your Roll No. on the top immediately on receipt of this question paper.)

Attempt **all** *questions.*
Parts of a question must be answered together.

1. (a) Show the bit configuration of a 24-cell register when it's content represents the decimal number 295 in BCD. (1)

   (b) Subtract $(10110.011)_2$ from $(11010.1)_2$ and verify the result by showing equivalent decimal substraction. (2)

   (c) What is a gray code ? (1)

2. (a) Show the dual of the exclusive – OR is equal to it's compement. (3)

   (b) A majority gate is a digital circuit whose output is equal to 1 if the majority of the inputs are 1s. The

P.T.O.

output is 0 otherwise. By means of a truth table, find the boolean function implemented by a 3-input majority gate. Simplify the function. (4)

(c) What is the usage of a buffer in a circuit ? (1)

(d) Simplify the boolean function given below by means of tabulation method.

$F(A, B, C, D, E, F, G) = \Sigma(20, 28, 38, 39, 52, 60, 102, 103, 127)$

(5)

3. (a) Design a circuit that detects an error in the representation of a decimal digit in BCD. In other words, obtain a logic diagram whose output is logic 1 when the inputs contain an unused combination in the code. (4)

(b) Using 4 exclusive – OR gates and a 4-bit full adders MSI circuit, construct 4-bit parallel adder/ subtractor. Use an input select variable 'V' so that when V = 0, the circuit adds and when V = 1, the circuit subtracts. (Hint : use 2's complement subtraction). (5)

(c) Design a circuit specified by 3 functions given below with a dual 4-line to 1-line multiplexer, an OR gate and an inverter

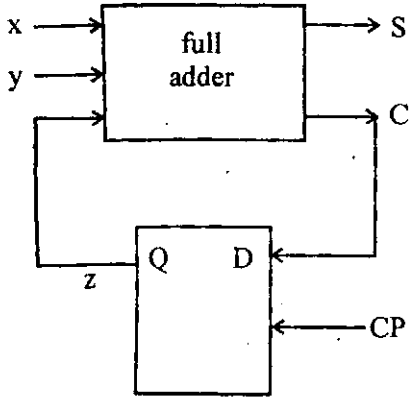
$F_1 = x'y' + xyz'$

$F_2 = x' + y$

$F_3 = xy + x'y'$ (4)

4. (a) A flip flop has a 20 nsec delay from the time it's clock pulse input goes from 1 to 0 to the time the output is complemented. What is the maximum delay in a 10-bit binary ripple counter that uses these flip flops ? What is the maximum frequency that the counter can operate at reliability ? (2)

(b) The full adder of given figure receives two external inputs x and y. The third input z comes from the output of a D flip flop. The carry output is transfered to the flip flop every clock pulse. The external output 'S' gives the sum x, y and z. Obtain the State Table and State Diagram of the sequential circuit (4)



(c) Design a BCD counter with JK flip flop. (6)

5. (a) Design a shift register with parallel load that operates according to the following table :

Shift	Load	Operation
0	0	No Change
0	1	Load 11 Data
1	X	Right Shift

(6)

(b) If the data at sender site is 1101, but received as 0101 at the receiver site, using Hamming code method show that bit no. 3 is in error. (5)

6. (a) Consider a sequential system that records (counts) the occurrence of 55 different events (numbered from 1 to 55), which take place one at a time. When the count of event i becomes a multiple of 100, the output z(t) = i, otherwise z(t) = 0. Obtain a state description of the system. (6)

(b) Determine the minimal state table equivalent to the following state table : (5)

Present State	Input			
	x = a	x = b	x = c	x = d
A	E, 1	C, 0	B, 1	E, 1
B	C, 0	F, 1	E, 1	B, 0
C	B, 1	A, 0	D, 1	F, 1
D	G, 0	F, 1	E, 1	B, 0
E	C, 0	F, 1	D, 1	E, 0
F	C, 1	F, 1	D, 0	H, 0
G	D, 1	A, 0	B, 1	F, 1
H	B, 1	C, 0	E, 1	F, 1
	NS, z			

7. (a) How many address inputs, data inputs and data outputs are required for 16K × 12 memory. (3)

(b) An asynchronous sequential circuit is described by the following excitation and output functions

$Y = X_1X_2' + (X_1 + X_2')Y$

$Z = Y$

(i) Derive the Transition table

(ii) Derive the Output map

(iii) Obtain the 2 state flow table (3)

(c) Using T flip flops, design a modulo-5 counter whose specification is :

Input : $x(t) \in \{0, 1\}$

Output : $z(t) \in \{0, 1, 2, 3, 4\}$

State : $s(t) \in \{S_0, S_1, S_2, S_3, S_4\}$

Initial state : $s(0) = S_0$

function : as specified by the following State Diagram (5)