

MOV - Opcode

E,M -Operand

5E -HEX code

1 -Bytes

Data Transfer Group		Arithmetic and logical group		Increment**(with Byte)		Logical* (With Bytes)	
Move(with byte)	Move immediate(with byte)	ADD* (with byte)					
MOV A, A 7F 1	MVI A, Data 3E 2	ADD A 87 1		INR A 3C 1		ANA A A7 1	
MOV A, B 78 1	MVI B, Data 06 2	ADD B 80 1	ADD C 81 1	INR B 04 1		ANA B A0 1	
MOV A, C 79 1	MVI C, Data 0E 2	ADD D 82 1		INR C 0C 1		ANA C A1 1	
MOV A, D 7A 1	MVI D, Data 16 2	ADD E 83 1		INR D 14 1		ANA D A2 1	
MOV A, E 7B 1	MVI E, Data 1E 2	ADD H 84 1		INR E 1C 1		ANA E A3 1	
MOV A, H 7C 1	MVI H, Data 26 2	ADD L 85 1		INR H 24 1	INR L 2C 1	ANA H A4 1	
MOV A, L 7D 1	MVI L, Data 2E 2	ADD M 86 1		INR M 34 1		ANA L A5 1	
MOVA, M 7E 1	MVI M, Data 36 2					ANA M A6 1	
MOV B, A 47 1							
MOV B, B 40 1	LXI	ADC(with byte)		INX(with byte)		XRA(with byte)	
MOV B, C 41 1		ADC A 8F 1		INX B 03 1	INX D 13 1	XRA A AF 1	
MOV B, D 42 1	Load	ADC B 88 1				XRA B A8 1	
MOV B, E 43 1	Immediate	ADC C 89 1		INX H 23 1		XRA C A9 1	
MOV B, H 44 1	B, dble 01	ADC D 8A 1		INX SP 33 1		XRA D AA 1	
MOV B, L 45 1	D, dble 11	ADC E 8B 1				XRA E AB 1	
MOV B, M 46 1	H, dble 21	ADC H 8C 1				XRA H AC 1	
MOV C, A 4F 1	SP, dble 31	ADC L 8D 1				XRA L AD 1	
MOV C, B 48 1		ADC M 8E 1				XRA M AE 1	
MOV C, C 49 1							
MOV C, D 4A 1							
MOV C, E 4B 1	Load/ Store *	Subtract*(with byte)		DCR(with byte) **		ORA(with byte)	
MOV C, H 4C 1		SUB A 97 1		DCR A 3D 1		ORA A B7 1	
MOV C, L 4D 1	LDAX B 0A	SUB B 90 1		DCR B 05 1		ORA B B0 1	
MOV C, M 4E 1	LDAX D 1A	SUB C 91 1		DCR C 0D 1		ORA C B1 1	
MOV D, A 57 1	LHLD adr2A	SUB D 92 1		DCR D 15 1		ORA D B2 1	
MOV D, B 50 1	LDA adr3A	SUB E 93 1		DCR E 1D 1		ORA E B3 1	
MOV D, C 51 1	STAX B 02	SUB H 94 1		DCR H 25 1		ORA H B4 1	
MOV D, D 52 1	STAX D 12	SUB L 95 1		DCR L 2D 1		ORA L B5 1	
MOV D, E 53 1	SHLD adr22	SUB M 96 1		DCR M 35 1		ORA M B6 1	
MOV D, H 54 1	STA adr 32						
MOV D, L 55 1							
MOV D, M 56 1		SBB(with byte)		DCX		CMP(with byte)	
MOV E, A 5F 1	XCHG	SBB A 9F 1		DCX B 0B		CMP A BF 1	
MOV E, B 58 1	XCHG EB	SBB B 98 1		DCX D 1B		CMP B B8 1	
MOV E, C 59 1		SBB C 99 1		DCX H 2B		CMP C B9 1	
MOV E, D 5A 1		SBB D 9A 1		DCX SP 3B		CMP D BA 1	
MOV E, E 5B 1		SBB E 9B 1				CMP E BB 1	
MOV E, H 5C 1		SBB H 9C 1				CMP H BC 1	
MOV E, L 5D 1		SBB L 9D 1				CMP L BD 1	
MOV E, M 5E 1		SBB M 9E 1				CMP M BE 1	
MOVH, A 67 1				Specials			
MOV H, B 60 1				DAA* 27			
MOV H, C 61 1				CMA 2F			
MOV H, D 62 1				STC† 37			
MOV H, E 63 1				CMC† 3F			
MOV H, H 64 1	byte = constact or logical/ arithmetic expression that evaluates to an 8-bit data quantity. (second byte of 2-byte instruction)	DAD(double add) †		Arith and Logical Immediate			
MOV H, L 65 1		DAD B 09 1		ADI byte C6			
MOV H, M 66 1		DAD D 19 1	DAD H 29 1	ACI byte CE			
MOV L, A 6F 1		DAD SP 39 1		SUI byte D6			
MOV L, B 68 1				SBI byte DE			
MOV L, C 69 1	dble = constant or logical/ arithmetic expression that evaluates to a 16-bit data quantity.(second and third bytes of 3-bytes instructions).			ANI byte E6			
MOV L, D 6A 1				XRI byte EE			
MOV L, E 6B 1				ORI byte F6			
MOV L, H 6C 1				CPI byte FE			
MOV L, L 6D 1							
MOV L, M 6E 1	adr= 16-bit address(second and third bytes of 3-byte instructions)						
MOV M, A 77 1	*= all flags (C, Z, S, P, AC) affected.			Rotate†			
MOV M, B 70 1	** = all flags except CARRY affected;			RLC 07			
MOV M, C 71 1	(except INX and DCX affect no flags).			RRC 0F			
MOV M, D 72 1	+ = only CARRY affected			RAL 17			
MOV M, E 73 1				RAR 1F			
MOV M, H 74 1							
MOV M, L 75 1							

8085 Instruction Summary by Functional Groups | 2

BRANCH CONTROL GROUP		I/O AND MACHINE CONTROL		ASSEMBLER REFERENCE	
JUMP		STACK	Ops	Pseudo Instructions	
JMP adr	C3	PUSH		General:	
JNZ adr JZ adr	C2				
JNC adr	CA	PUSH B	C5	ORG	
JC adr	D2	PUSH D	D5 E5	END	
JPO adr	DA	PUSH H	F5	EQU	
JPE adr	E2	PUSH PSW		SET	
JP adr	EA			DS	
JM adr	F2			DB	
PCHL	FA			DW	
	E9				
CALL		POP		MACROS:	
CALL adr CD		POP B	C1	MACRO	
CNZ adr C4		POP D	D1	ENDM	
CZ adr CC		POP H	E1	LOCAL	
CNC adr D4		POP PSW*	F1	REPT	
CC adr DC				IRP	
CPO adr E4 CPE adr EC		XTHL SPHL	E3 F9	IRPC	
CP adr F4				EXITM	
CM adr FC					
Return		Input/Output		Relocation:	
RET	C9	OUT byte IN byte	D3 DB	ASEG	
RNZ RZ	C0			DSEF	
RNC	C8	Control		CSEF	
RC	D0			PUBLIC	
RPO	D8			EXTRN	
RPE	E0	DI	F3		
RP	E8	EI	FB		
RM	F0	NOP	00		
	F8	HLT	76		
		New Instructions (8085 only)		Conditional Assembly:	
		RIM SIM	20	IF	
			30	ELSE	
				ENDIF	
		RESTART TABLE			
Restart		Name	Code	Restart Address	
RST0	C7	RST 0	C7	0000H	
RST1	CF	RST 1	CF	0008H	
RST2	D7	RST 2	D7	0010H	
RST3	DF	RST 3	DF	0018H	
RST4	E7	RST 4	E7	0020H	
RST5	EF	TRAP	Hardware* Function	0024H	
RST6	F7	RST 5	EF	0028H	
RST7	FF	RST 5 5 RST 6	Hardware* Function	002CH	
		RST 6 5 RST 7	F7	003BH	
		RST 7 5	Hardware* Function	003CH	
			FF		
			Hardware* Function		

*NOTE The hardware functions refer to the on-chip interrupt feature of the 8085 only

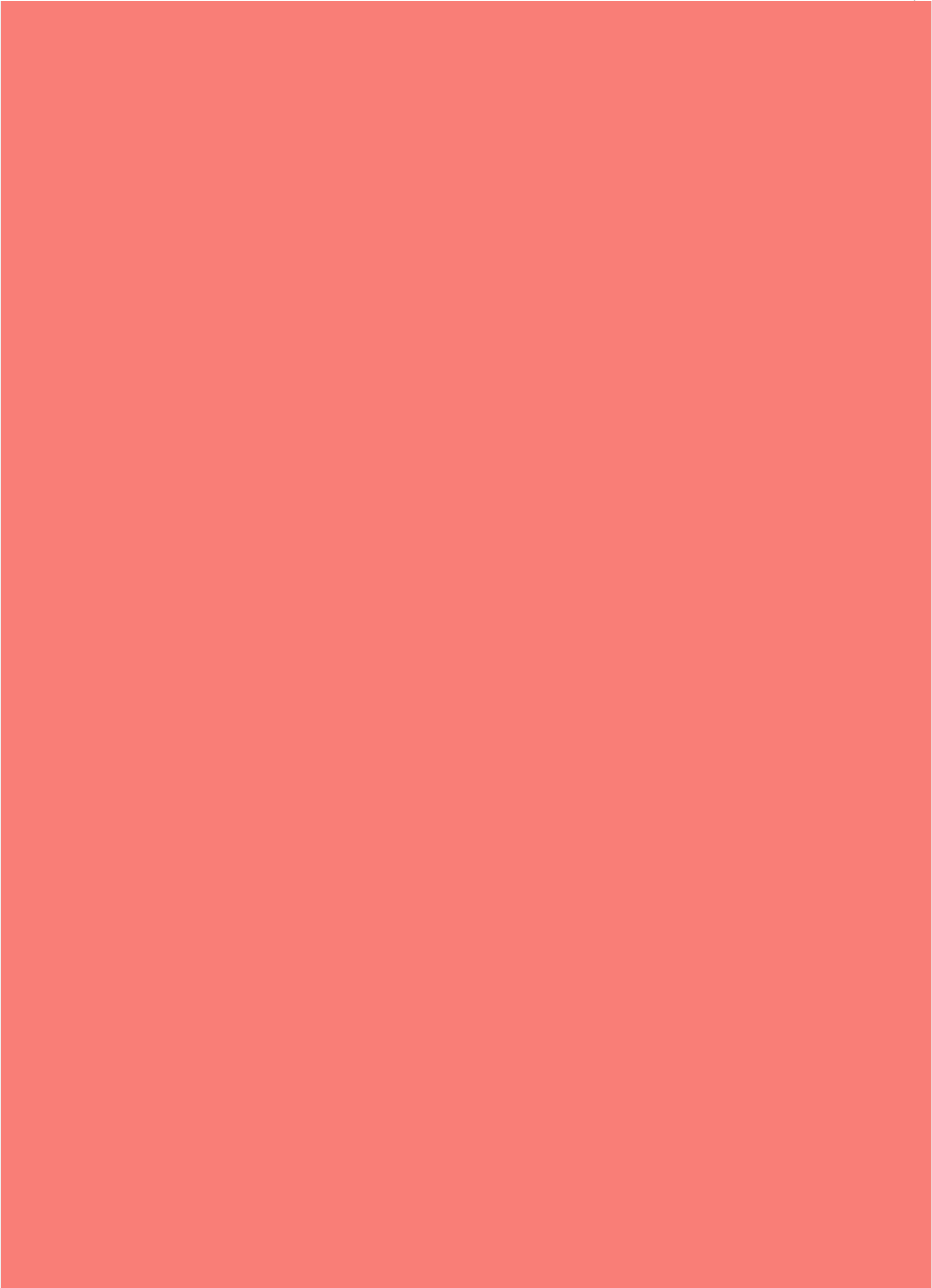


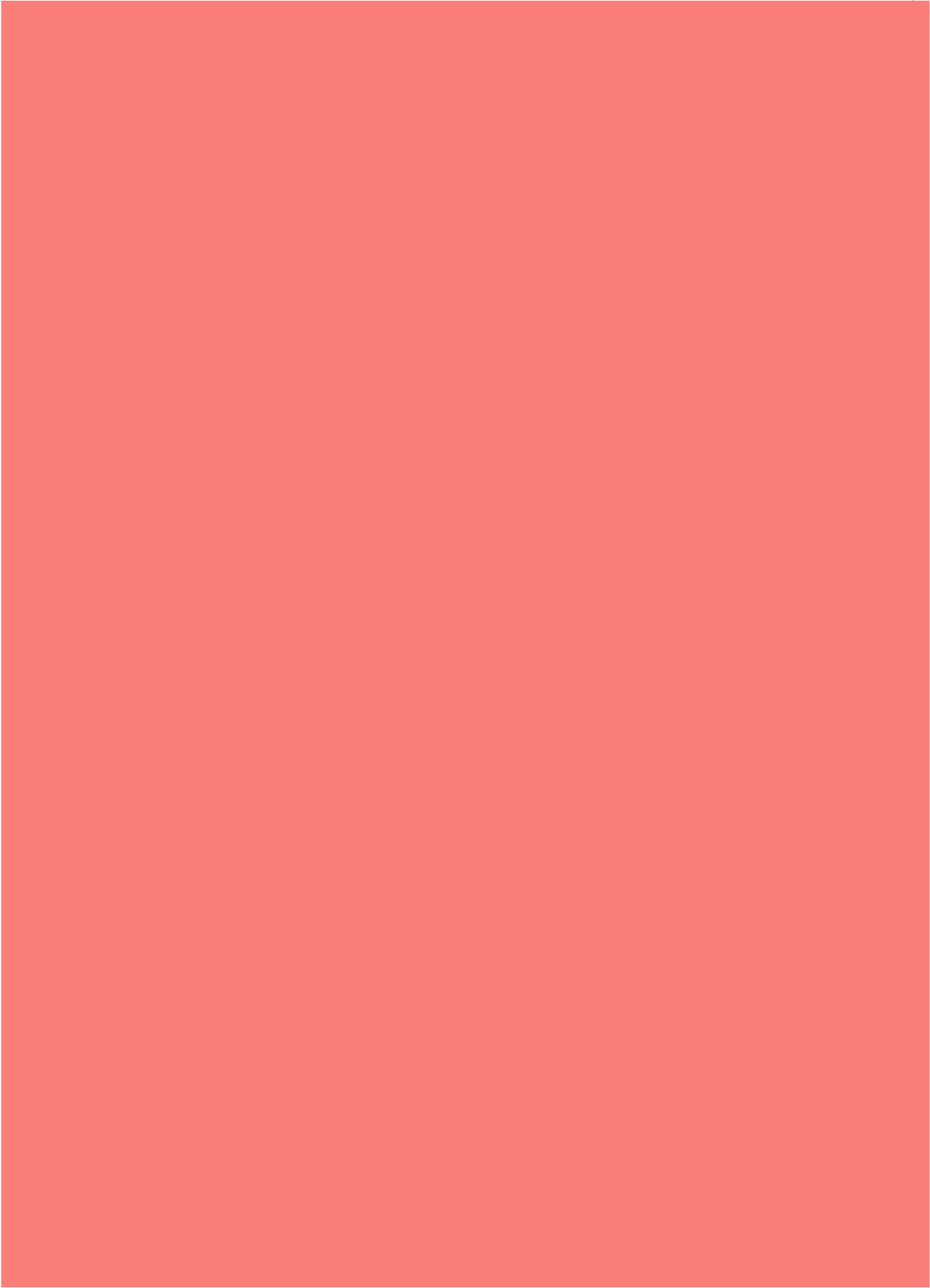
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I'm a physicist specializing in computational material science with a PhD in Physics from Friedrich-Schiller University Jena, Germany. I write efficient codes for simulating light-matter interactions at atomic scales. I like to develop Physics, DFT, and Machine Learning related apps and software from time

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